# Development of impedance matching circuit for coupling of Planar Multijunction Thermal Converters to Programmable Josephson Voltage Standards

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**Abstract**. With the SI redefinition, back in May 20th, 2019, any method capable of deriving a SI base quantity value traceable to the set of seven reference constants, could be used to realize their respective SI unit (stricto sensu realization). This is the case of the volt realized through Josephson Voltage Standards (JVS). Although such systems are widely used for dc voltage sources and meters calibration, their application in ac voltage calibrations still have some limitations (in amplitude range, frequency range, etc.). Hence, Thermal Converters (TC) still play an important role in the AC voltage calibration field. However, TC calibration is not directly linked to the new SI fundamental constants, which could be provided by JVS. Such primary standards, on the other hand, do not provide currents big enough for Thermal Converters calibration (for instance, 7.5 mA, as it is the case of Planar Multijunction Thermal Converters – PMJTC – with 400 Ω of input resistance and 3 V maximum input voltage). Hence, we developed an impedance matching circuit, for coupling of PMJTC to Programmable Josephson Voltage Standards (PJVS), aiming to establish a link between the Josephson AC primary standard voltage system and the AC-DC transfer standard. We investigated potential operational amplifiers proper for such applications and four integrated circuits were chosen. Among the topologies previously studied, simulations and assembly of impedance matching circuits prototypes were made, and the one that behaved best in the required function presented an approximate average error of -1.51 μV and Type A uncertainty of 0.07 μV/V.

## 1. Introduction

Electricity is the most widely used way of energy in today's society, supporting for industrial development and other technological branches. In order to develop and repair circuits and alternating voltage (AC) equipments, power supplies and measuring instruments are used, whose voltages and measures have to be reliable, requiring that they are calibrated by comparison with reference standards. Metrological traceability is the property of the result of a value measurement with a standard related to established references, usually to national or international standards, through a continuous chain of comparisons.

The electrical voltage quantity is realized based on the Josephson effect, using a Josephson Voltage System in direct voltage (DC) [1]. Direct calibration of alternating electrical voltage sources is done through standard AC voltage meters. Josephson systems can also be used to directly calibrate AC voltage sources. At Inmetro, the classical calibration of alternating electrical voltage sources currently, goes through thermal converters (TCs) which has its traceability starting from a National Metrology Institute (Physikalisch Technische Bundesanstalt - PTB). One of the main goals of this ongoing research is to achieve independence in obtaining traceability in AC voltage.

Traceability in AC voltage comes from traceability in DC voltage through Josephson systems combined with traceability in AC-DC transfer by thermal converters [2]. This traceability currently depends on calibration by artefact-based standards and the proposal is aligned with the redefinition of the SI, in which fundamental physical constants must be used to obtain traceability in AC-DC transfer quantity. Programmable Josephson Voltage Standard (PJVS) is a standard voltage source, which uses the technology of grouping superconducting junctions on a chip, based on the Josephson effect, having good noise immunity, good operability and stable output voltage, being able to synthesize DC and AC signals [3]. Planar Multijunction Thermal Converter (PMJTC) is an AC-DC transfer standard, which compares the heating effect generated by an unknown AC signal with a known (and traceable to the SI) DC signal consisting of a heating element and a sensing thermal element by thermal coupling. The use of an impedance matching circuit is necessary, in order to allow calibration of the thermal converter (TC) using the Josephson standard, as well as to supply the electrical current required by the resistive load of this circuit [4].

## 2. Impedance matching circuit

The AC Josephson Programmable Voltage Standards (PJVS systems generating AC voltages) can only operate with small loads, that is, high resistances connected to their outputs so it is necessary to use fast electronic amplifiers (buffers) to provide the corresponding impedance and to allow that AC-DC transfer measurements can be made in the proposed system, as presented in Figure 1.

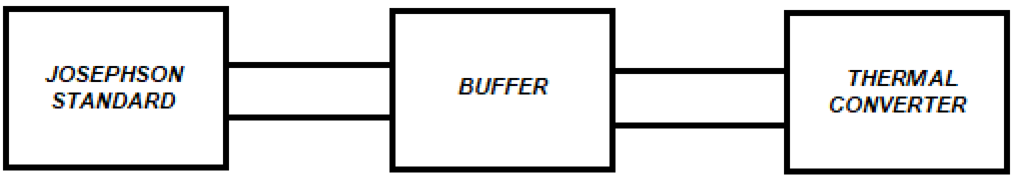


**Figure 1.** Proposed system

We have investigated some topologies of impedance matching circuits (buffers), using operational amplifiers, in order to allow the connection of PJVS to PMJTC. After conducting preliminary tests, we opted to concentrate on the classic voltage follower (topology A), presented in Figure 2 (a) [5], and on a voltage follower with six transistosr in push-pull configuration (topology B), shown in Figure 2 (b) [6]. The voltage follower buffer has the following characteristics: less influence on the results of errors and uncertainties in measurements of the signal generated by the PJVS and delivered to TC due to using fewer electronic components, current gain limited by the operational amplifier used, low noise. The push-pull buffer with six transistors has greater current amplification, greater amplification stability of positive and negative signals (AC and DC), greater bandwidth of operating frequencies.

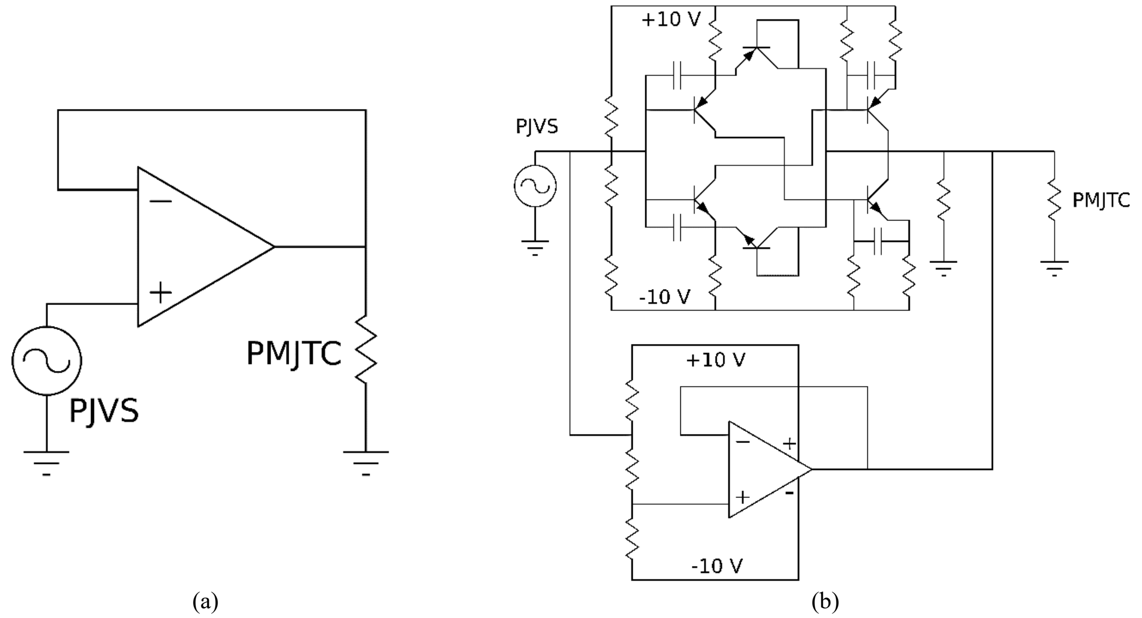


**Figure 2.** Simple voltage follower (a) and buffer push-pull with six transistors (b).

We have investigated some operational amplifiers, with the purpose of their use in the above mentioned impedance matching circuit. Among them the integrated circuits LF351 (National), AD844 (Analog Devices), LM6171 (Texas Instruments) and OP07 (Analog Devices) stood out, which have high input impedances to require low electrical current from the PJVS output, as required by this application, ultra-low offset voltage to generate smaller errors, output current capable of supplying the TC load, large frequency band, large slew rate.

## 3. Simulation

Simulations of buffer circuits were made in the Linear Technology's Ltspice simulation software. In order to evaluate DC gain linearity a DC voltage sweep simulation was performed using ramped signal source from -3 V to 3 V amplitude with $10^6$ points of resolution and 6 µV increments. Such signal was, compared to the output obtained experimentally by simulation with the mathematical model, Equation (1) of the straight line with the gain and the offset [6].

A linear regression was performed comparing these experimental results with the expected results through the model, leading to the calculation of the error and uncertainty of the circuit. Good DC gain linearity is important for AC-DC comparisons, even at low frequencies. The gain of an amplifier must be constant, so the output voltage is as follows:

$$V_{out\ calc} = a * V_{in} + b \qquad (1)$$

where $V_{out\ calc}$ is the calculated output voltage, $V_{in}$ is the input voltage, $a$ is the gain, and $b$ is the offset [6].

The results for DC gain linearity were obtained by subtracting the linearized buffer gain from the output voltage. The voltage sweep was performed in several voltage values to detect any non linear trends in gain. The loads were chosen to simulate the TCs used for equivalent measurements of the AC-DC difference [6].

Six buffer circuits were tested with satisfactory results, as follows: four based on topology A, according Figure 2 (a), with integrated circuits LM6171, AD844, LF351 and OP07; and, two based on topology B, as shown in Figure 2 (b), with integrated circuits LM6171 and AD844.

Based on simulation results, linear regressions were performed to find the gains and offsets, calculating the linearized gains of the buffers, according to the Equation (1), finding their errors, standard deviations and type A uncertainties, all registered in the generated sheets. Error graphs for the linearization of DC gain were also generated using Excel for every simulation conducted.

The objective of using linear regression in the spreadsheet generated in the MS Excel software is to obtain a mathematical model that best fits the observed values of the output voltage of the circuit ($V_{out}$) as a function of the variation of the levels of its input voltage ($V_{in}$), thus finding the gain and offset to calculate the new output voltage ($V_{out\ calc}$) through Equation (2), and find the error (*Error)* with the subtraction of the simulated original output voltage ($V_{out}$), represented in the relation:

$$Error = V_{out} - V_{out\ calc} \qquad (2)$$

Then the standard deviation and Type A uncertainty of the simulated buffer circuit are calculated.

In buffer topologies with six transistors in push-pull, the circuit that presented the best behavior was the one that used AD844 integrated circuit because it obtained an average error of 0.012 µV/V and a type A uncertainty of 0.013 µV/V, as presented in Table 1.

In the voltage follower buffer topologies, the circuit that obtained the best results was one that used the OP07 integrated circuit, with an average error of $-4.10^{-9}$ µV/V and a type A uncertainty of 0.003 µV/V, as presented in Table 1. As depicted in Figure 3, one can observe a high level of linearity of the voltage follower circuit with OP07.

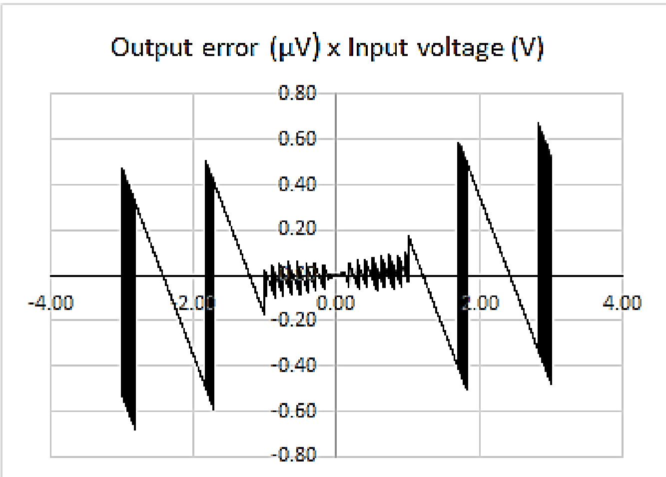


**Figure 3.** Output error x input voltage graph of the voltage follower circuit with OP07

Calculated errors and Type A uncertainties resulting in p.p.m. order (µV/V), as shown in Table 1.

**Table 1.** Simulation results.

| Buffer circuit topology | Average error (µV/V) | Uncertainty A (µV/V) |
|---|---|---|
| Push-pull with six transistor and LM6171 | -0.022 | 0.014 |
| Push-pull with six transistors and AD844 | 0.012 | 0.013 |
| Voltage follower with LM6171 | -0.006 | 0.01 |
| Voltage follower with AD844 | -0.0001 | 0.003 |
| Voltage follower with LF351 | 0.005 | 0.003 |
| Voltage follower with OP07 | $-4.10^{-9}$ | 0.003 |

## 4. Assembly and tests

Prototypes of the buffer circuits cited above were assembled on Printed Circuit Boards (PCBs), and were tested at Inmetro, through automated measurements using a Python language-based program, in a GPIB instrumentation network, controlling a FLUKE 5720A model calibrator, used as voltage source, and a KEYSIGHT 3458A model digital multimeter, as shown in Figure 4.

## 5. DC signal tests

The assembled circuits were fed at their inputs, using DC voltage ramp signal from -3 V to 3 V, as mentioned in Section 3, and they were tested with the measurement system shown in Figure 4.

According to the tests performed and the results obtained, we could conclude that the buffer circuit prototypes that presented the best performances were: (a) the classic voltage follower using the integrated circuit operational amplifier LF351, which presented an average error of approximately 3.56 µV and a type A uncertainty of 1.58 µV/V; and (b) the classic voltage follower using the OP07 operational amplifier integrated circuit, who presented an average error of approximately -1.62 µV and a type A uncertainty of 0.78 µV/V, indicating them with the best performances and who were closest to the goals of this research.

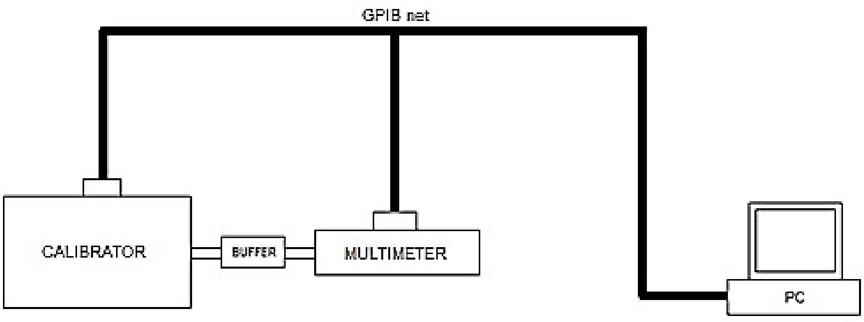


**Figure 4.** Buffer stability measurement system

## 6. AC signal tests

Automated measurements of the voltage-follower buffer circuit with the integrated circuits LF351 and OP07 were performed in order to analyze the behavior of the circuit being fed by electrical voltage signals in alternating form, in which the input signal used was 3 V at a frequency of 100 Hz generated by a FLUKE calibrator, the output signal was measured by a digital multimeter, previously reported and also shown in Figure 4.

The test results showed that the voltage-follower buffer circuit using the OP07 operational amplifier, with offset voltage compensation, was the best option amongst the buffer circuit prototypes tested. It presented, an average error value of 1.52 µV and its type A uncertainty was 0.07 µV/V. For comparison purposes, using the same topology with the LF351 operational amplifier, also with offset voltage compensation, the average error was 24 µV with a type A uncertainty of 2.01 µV/V.

## 7. Measurement of AC-DC differences

In order to evaluate the buffer performance in AC-DC transfer difference, several measurements were made using thermal converters (TCs) at Inmetro [7].

The measurement system (Figure 5) consists of a DC Source and an AC Source (both implemented using a Fluke calibrators), two Keithley (182 model) nanovoltmeters used to measure the thermal converters outputs and an automated switch. The system is fully automated, controlled by a custom made software. In this measurement system, the reference standard TC and the device under test TC are connected in parallel, and a sequence of AC, DC (direct), AC, DC (reverse) and AC input voltages are applied by the measuring software. The output voltages of both TCs is recorded and used to calculate the AC-DC transfer difference.

The reference standard is a 90 ohm PMJTC traceable to PTB. The device under test is a 90 ohm Single Junction Thermal Converter (SJTC).

The measurements were performed at 3 V voltage level, 100 Hz frequecy.

We measured the AC-DC transfer difference of the SJTC alone (without the buffer) and then we repeated the measurements with the buffer connected to the input of the SJTC, in order to evaluate the AC-DC transfer difference introduced by the buffer. The results are shown in Table 2, in which confirms that the OP07 integrated circuit obtained better results than the LF351.

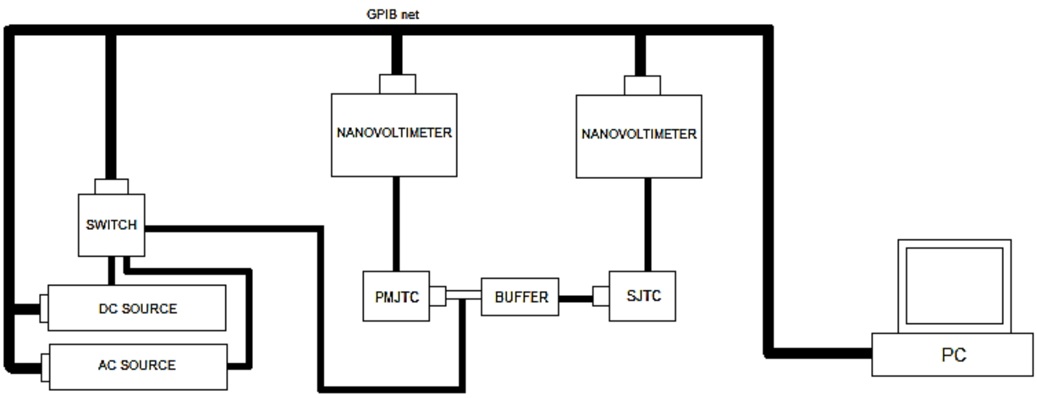


**Figure 5.** Buffer AC-DC differences measurement system

**Table 2.** AC-DC differences results

| Buffer | $V_{IN}$ (V) | Frequency (Hz) | Average (µV/V) | Standard deviation (µV/V) |
|---|---|---|---|---|
| No buffer | 3 | 100 | 5.33 | 0.98 |
| LF351 | 3 | 100 | 25.00 | 2.14 |
| OP07 | 3 | 100 | 4.05 | 1.20 |

## 8. Arbitrary signal tests

In order to verify the behavior of the buffer circuit, fed by a signal similar to that generated by the PJVS, an arbitrary waveform generator KEYSIGHT 33600A model was configured, with seven files of arbitrary signals for the resolutions of 32, 64, 128, 256, 512, 1024 and 2048 steps.

Automated measurements were made of signals generated by the arbitrary waveform generator initially with no buffer. Also, these measurements were repeated using a circuit including the voltage follower buffer with OP07, its results are shown in Table 3. Both, circuits were excited by arbitrary 3 V signals at a frequency of 100 Hz, and the output signal was measured by a KEYSIGHT 3458A digital multimeter, as shown in Figures 6 and 7.

**Table 3.** Buffer results with OP07 for $V_{OUT}$ = 3 VRMS / 100 Hz

| Resolution (steps) | Average (V) | Average error (µV) | Standard deviation (µV/V) | Type A Uncertainty (µV/V) |
|---|---|---|---|---|
| 32 | 2.999810999 | -189.00 | 87.54 | 8.75 |
| 64 | 2.999839993 | -160.01 | 76.35 | 7.64 |
| 128 | 3.000048238 | 48.24 | 95.36 | 9.54 |
| 256 | 2.999890939 | -109.06 | 121.70 | 12.17 |
| 512 | 2.999537413 | -462.59 | 91.35 | 9.13 |
| 1024 | 2.999490826 | -509.17 | 67.30 | 6.73 |
| 2048 | 2.999485505 | -514.50 | 91.52 | 9.15 |

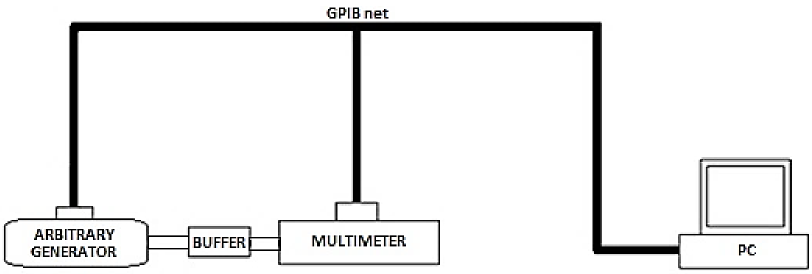


**Figure 6.** Measurement system with arbitrary waveform generator

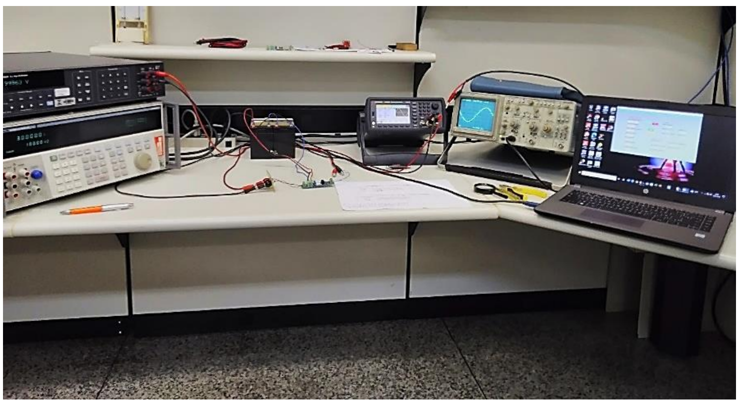

**Figure 7.** Measuring system with arbitrary waveform generator in operation

According to the analysis carried out on the results presented in tables 3, the graphs in Figure 8 below were generated, in which the configurations that presented the best average error and Type A uncertainty ratios were one with 512 steps for the one that used only the arbitrary waveform generator, which obtained the error of -3187.46 μV and uncertainty of 8.23 μV/V, and the one with 128 steps that used the buffer OP07 at the output of the arbitrary waveform generator, which obtained an error of 48.24 μV with a Type A uncertainty of 9.54 μV/V.

Due to the natural gain of the operational amplifier integrated circuit used, smaller errors occurred than those found with measurements carried out only with arbitrary waveform generator, thus ending the tests related to this research.

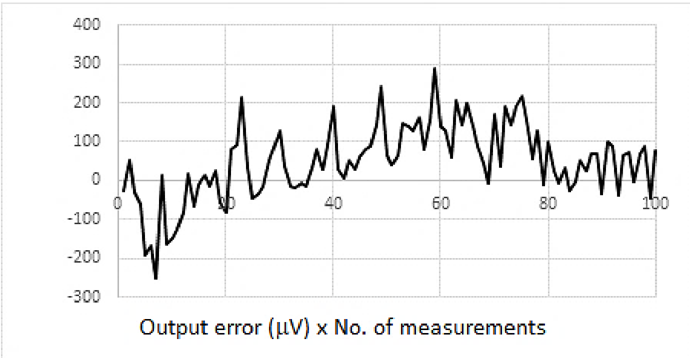


**Figure 8.** OP07 buffer output error with 128 step input signal

## 9. Conclusion

In this work, we carried out some studies, surveys, acquisition of electronic components, parts, tools and measuring instruments, electronic circuit simulator software, assemblies and tests of buffer prototypes. The discrepancy verified between the results obtained from the measurements made in buffer circuits tested, in computer simulations and in tests using assembled circuits and instruments of measurement labotories, happened due to their differences in metrological parameters, and by the influence of the geometry of installation of the measurement systems, considering that the respective results were obtained in order of ppm.

According to the results obtained, topologies of voltage-following buffer circuits were chosen to be assembled, using operational amplifiers with high input impedance and high precision with ultra-low offset voltage values, such as the OP07 circuit which obtained the best results, and achieved average error values of 48.24 μV, Type A uncertainty of 9.54 μV/V, low input currents of 65.18 pA, and output current capability above 20.00 mA, finding technical prerequisites for connecting the standard voltage electrical (PJVS) to the thermal converter (PMJTC), object of this research, and thus make possible an alternative for the calibration of PMJTC by PJVS, in the standardization of alternating electrical voltage.

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